اسم المقرر: الدارات المنطقية | اليوم و التاريخ: الأحد 2019/01/06 | الفترة الإمتحانية: الأولى

عدد الصفحات: 5 | عدد الاسئلة: 7 | الدرجة: خمسون | مدة الامتحان: ساعة ونصف

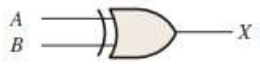
اسم المدرس: د. م. حسـان أحمـد | العام الدراسي: 2018- 2019 | الفصل: الأول

Part _I. Choose the correct answer: [25 marks]

1.	**The number of values that can be assigned to a bit are**			
	A. two	B. ten	C. eight	D. one
2.	**AND, OR, and NOT gates can be used to form**			
	A. storage devices	B. all answers (A,C,D)	C. comparators	D. data selectors
3.	**A shift register is an example of a**			
	A. comparator	B. counter	C. storage device	D. data selector
4.	**A device that is used to switch one of several input lines to a single output line is called a**			
	A. comparator	B. decoder	C. demultiplexer	D. multiplexer
5.	**The binary number 11011101 is equal to the decimal number**			
	A. 221	B. 121	C. 321	D. 212
6.	**The decimal number 250 is equivalent to the binary number**			
	A. 11110110	B. 11111010	C. 11111000	D. 11111011
7.	**The 2's complement of 11001100 is**			
	A. 00110011	B. 00110101	C. 00110100	D. 00110110
8.	**The decimal number –234 is expressed in the 2's complement form as**			
	A. 01011110	B. 10100010	C. 01011101	D. 11011110
9.	**An inverter performs an operation known as**			
	A. both answers (B) and (C)	B. complementation	C. inversion	D. all answers (A,B,C) are valid
10.	**A Boolean expression that is in standard SOP form is**			
	A. the minimum logic expression	B. has every variable in the domain in every term	C. contains only one product term	D. all answers (A,B,C) are valid
11.	**Adjacent cells on a Karnaugh map differ from each other by**			
	A. two variables	B. all variables	C. one variable	D. answer depends on the size of the map
12.	**A variable is a symbol in Boolean algebra used to represent**			
	A. data	B. a condition	C. an action	D. answers A, B, and C
13.	The Boolean expression $\overline{ABCD}$ is			
	A. a product term	B. an inverse term	C. a literal term	D. all answers (A,B,C) are valid
14.	Which one of the following is not a valid rule of Boolean algebra?			
	A. $A + 1 = 1$	B. $A = \overline{A}$	C. $AA = A$	D. $A + 0 = A$
15.	According to DeMorgan's theorems, the complement of a product of variables is equal to			
	A. the complement of the sum	B. the product of the complements	C. the sum of the complements	D. answers A, B, and C

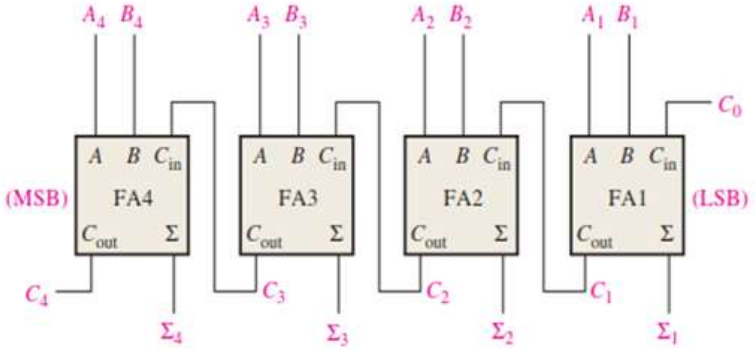
16.	Decoder is a digital circuit that converts coded information into a			
	A. noncoded form	B. coded form	C. specified form	D. all answers (A,B,C) are not valid
17.	Encoder a digital circuit that converts information to a coded form			
	A. noncoded form	B. coded form	C. specified form	D. all answers (A,B,C) are not valid
18.	Full-adder a digital circuit that adds two bits and an input carry to produce a			
	A. sum output only	B. output carry only	C. sum and an output carry	D. all answers (A,B,C) are valid
19.	Multiplexer is a circuit that switches digital data from several input lines onto a			
	A. single output line	B. multi single output line	C. several single output line	D. all answers (A,B,C) are valid
20.	An active HIGH input S-R latch is formed by the cross-coupling of			
	A. two NAND gates	B. two NOR gates	C. two OR gates	D. two AND gates
21.	A flip-flop changes its state during the			
	A. falling edge of the clock pulse	B. rising edge of the clock pulse	C. both answers (A) and (B)	D. all answers (A,B,C) are not valid
22.	For an edge-triggered D flip-flop,			
	A. a change in the state of the flip-flop can occur only at a clock pulse edge	B. the state that the flip-flop goes to depends on the D input	C. the output follows the input at each clock pulse	D. all answers (A,B,C) are valid
23.	J-K flip-flop is SET when			
	A. J = 1, K = 1	B. J = 0, K = 0	C. J = 0, K = 1	D. J = 1, K = 0
24.	A register's functions include			
	A. data storage	B. data movement	C. neither (a) not (b)	D. both (a) and (b)
25.	To enter a byte of data serially into an 8-bit shift register, there must be			
	A. one clock pulse	B. two clock pulses	C. four clock pulses	D. eight clock pulses

Part II. Solve each of the following problems

1.	For the Exclusive-OR gate, write the Boolean expression and construct its truth table. **[4 marks]** 
2.	Apply DeMorgan's theorems to each expression: **[4 marks]** a. $\overline{A(B+C)}$ b. $\overline{(A+\overline{B})(\overline{C}+D)}$
3.	Use a Karnaugh map to minimize the following standard SOP expression: **[4 marks]** $A\overline{B}C+\overline{A}BC+\overline{A}\,\overline{B}C+\overline{A}\,\overline{B}\,\overline{C}+A\overline{B}\,\overline{C}$

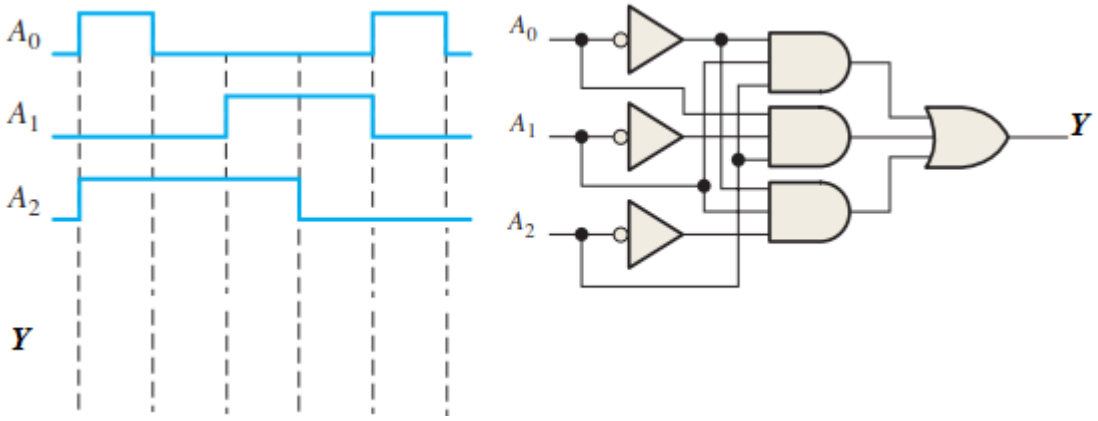
4. The following sequences of bits (right-most bit first) appear on the inputs to a 4-bit parallel adder shown in Fig. Determine the resulting sequence of bits on each sum output. **[4 marks]**

A_1	1010
A_2	1100
A_3	0101
A_4	1101
B_1	1001
B_2	1011
B_3	0000
B_4	0001



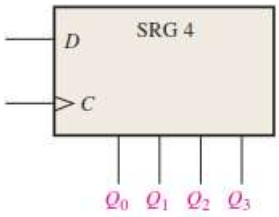
5. If the input waveforms are applied to the decoding logic as indicated in Figure: **[4 marks]**

a. Write the output Boolean expression for ***Y***;
b. Sketch the output waveform in proper relation to the inputs.



6. Given the 4-bit register (SRG 4) in Figure. **[5 marks]**

a. Give the name of the type of this register;
b. Show the states of the register for the data input and clock waveforms in Figure. Assume that the register initially contains all 1s.



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With best success Dr. Eng. Hassan Ahmad